Claims:

1. A power management system for a computer system having one or more different components wherein power is dynamically supplied to each component, the power management system comprising:

a clock generator circuit for generating one or more different clock signals wherein each clock signal has a different predetermined frequency;

a clock selector circuit that, based on the task being performed by the computer system, dynamically adjusts the clock signal supplied to each component of the computer system in order to reduce the total power being consumed by the computer system.

2. The system of Claim 1 further comprising a static power management system wherein power is withdrawn from components that are not currently active to reduce the power consumption of the computer system.

3. The system of Claim 2, wherein the static power management system further comprises a circuit for disconnecting the address, control data in and data out pins of a component of the computer system in order to reduce the power consumption of the computer system.

4. The system of Claim 1, wherein the clock generator circuit further comprises a first oscillator that generates a first clock signal, a second clock oscillator that generates a second clock signal, a programmable clock circuit that generates a third clock signal based on the second clock signal, and a clock select circuit that selects one of the first, second and third clock signal that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock signal.

5. The system of Claim 4, wherein the clock select circuit further comprises a clock state machine for determining the clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the clock select circuit in order to output the appropriate clock signal.

6. The system of Claim 5, wherein the clock state machine further comprises an idle state wherein the computer system is waiting for an input, a busy state wherein the computer

system is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

7. The system of Claim 6, wherein the clock select circuit further comprises a circuit that generates a system clock, a circuit that generates a processor clock and a circuit that generates a co-processor clock wherein each of the clocks is independently and simultaneously.

8. The system of Claim 6, wherein, during the idle state, the clock select circuit generates no clock for the phase locked loop and co-processor so that they are off, the clock select circuit generates the first clock signal for the processor so that the processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system quickly.

9. The system of Claim 6, wherein, during the busy state, the clock select circuit generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

10. The system of Claim 6, wherein, during the sleep state, the clock select circuit generates no clock signal for the processor and the co-processor.

11. The system of Claim 5, wherein the clock state machine is controlled by an interrupt signal and software commands.

12. The system of Claim 4, wherein the programmable clock circuit generates a fourth clock signal.

13. The system of Claim 12, wherein the first, second, third and fourth clock signals have different frequencies.

14. The system of Claim 13, wherein the first clock signal frequency comprises 32 kHz, the second clock signal frequency comprises 24 MhZ, the third clock signal frequency comprises 33 MhZ and the fourth clock signal frequency comprises 66 MhZ.

15. The system of Claim 4 further comprises a time of day circuit that generates time of day clock signals based on the first clock signal.

16. The system of Claim 4, wherein the clock select circuit further comprises means for dynamically changing the clock frequency applied to each component of the computer system based on the task being performed by the computer system.

17. The system of Claim 4, wherein the clock select circuit comprises a multiplexer.

18. The system of Claim 4, wherein the programmable clock generator further comprises a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

19. A power management method for a computer system having one or more different components wherein power is dynamically supplied to each component, the power management method comprising:

simultaneously generating one or more different clock signals wherein each clock signal has a different predetermined frequency;

dynamically adjusts the clock signal supplied to each component of the computer system in order to reduce the total power being consumed by the computer system.

20. The method of Claim 19 further comprising static power management method wherein power is withdrawn from components that are not currently active to reduce the power consumption of the computer method.

21. The method of Claim 20, wherein the static power management further comprises disconnecting the address, control data in and data out pins of a component of the computer method in order to reduce the power consumption of the computer method.

22. The method of Claim 19, wherein the clock generation further comprises generating a first clock signal with a first oscillator, generating a second clock signal using a second oscillator, generating a third clock signal based on the second clock signal, and selecting one of the first, second and third clock signal that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock signal.

23. The method of Claim 22, wherein the clock select further comprises determining the clock state of the computer system at a predetermined time and generating control signals to the clock select in order to output the appropriate clock signal.

24. The method of Claim 23, wherein the clock state machine further comprises an idle state wherein the computer method is waiting for an input, a busy state wherein the computer method is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

25. The method of Claim 24, wherein the clock select circuit further comprises generating a system clock, generating a processor clock and generating a co-processor clock wherein each of the clocks is independently and simultaneously.

26. The method of Claim 24, during the idle state, generating no clock for the phase locked loop and co-processor so that they are off, generating the first clock signal for the processor so that the processor is clocked at a slow rate and generating a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer method quickly.

27. The method of Claim 24, during the busy state, generating a high rate clock signal for the processor, the co-processor and the interrupt circuits.

28. The method of Claim 24, during the sleep state, generating no clock signal for the processor and the co-processor.

29. The method of Claim 23, wherein the clock state machine is controlled by an interrupt signal and software commands.

30. The method of Claim 22 further comprising generating a fourth clock signal.

31. The method of Claim 30, wherein the first, second, third and fourth clock signals have different frequencies.

32. The method of Claim 31, wherein the first clock signal frequency comprises 32 kHz, the second clock signal frequency comprises 24 MhZ, the third clock signal frequency comprises 33 MhZ and the fourth clock signal frequency comprises 66 MhZ.

33. The method of Claim 22 further comprises a time of day circuit that generates time of day clock signals based on the first clock signal.

34. The method of Claim 22, wherein the clock select circuit further comprises means for dynamically changing the clock frequency applied to each component of the computer method based on the task being performed by the computer method.

35. The method of Claim 22, wherein the clock select circuit comprises a multiplexer.

36. The method of Claim 22, wherein the programmable clock method further comprises a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

37. A flexible clock generator, comprising:

a first oscillator that generates a first clock signal;

a second clock oscillator that generates a second clock signal;

a programmable clock circuit that generates a third clock signal based on the second clock signal; and

a clock select circuit that selects one of the first, second and third clock signal that is supplied to a portion of the computer system to provide that portion of the computer system with a predetermined clock signal.

38. The generator of Claim 37, wherein the clock select circuit further comprises a clock state machine for determining the clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the clock select circuit in order to output the appropriate clock signal.

39. The generator of Claim 38, wherein the clock state machine further comprises an idle state wherein the computer system is waiting for an input, a busy state wherein the computer system is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power has failed to the computer system.

40. The generator of Claim 39, wherein the clock select circuit further comprises a circuit that generates a system clock, a circuit that generates a processor clock and a circuit that generates a co-processor clock wherein each of the clocks is independently and simultaneously.

41. The generator of Claim 39, wherein, during the idle state, the clock select circuit generates no clock for the phase locked loop and co-processor so that they are off, the clock select circuit generates the first clock signal for the processor so that the processor is clocked at a slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system quickly.

42. The generator of Claim 39, wherein, during the busy state, the clock select circuit generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

43. The generator of Claim 39, wherein, during the sleep state, the clock select circuit generates no clock signal for the processor and the co-processor.

44. The generator of Claim 38, wherein the clock state machine is controlled by an interrupt signal and software commands.

45. The generator of Claim 37, wherein the programmable clock circuit generates a fourth clock signal.

46. The generator of Claim 45, wherein the first, second, third and fourth clock signals have different frequencies.

47. The generator of Claim 46, wherein the first clock signal frequency comprises 32 kHz, the second clock signal frequency comprises 24 MhZ, the third clock signal frequency comprises 33 MhZ and the fourth clock signal frequency comprises 66 MhZ.

48. The generator of Claim 37 further comprises a time of day circuit that generates time of day clock signals based on the first clock signal.

49. The generator of Claim 37, wherein the clock select circuit further comprises means for dynamically changing the clock frequency applied to each component of the computer system based on the task being performed by the computer system.

50. The generator of Claim 37, wherein the clock select circuit comprises a multiplexer.

51. The generator of Claim 37, wherein the programmable clock generator further comprises a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.